LOW IMPEDANCE MEMORY BITLINE ELIMINATING PRECHARGE

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ABSTRACT OF THE DISCLOSURE

[031] A memory system using low impedance memory bitlines that eliminate the need for a precharge clock signal. An equilibration circuit controlled by a reference voltage is connected to the first and second bitlines of a memory cell and is operable to maintain a predetermined equilibrium condition between the first and second bit lines. The equilibration circuit is operable to generate an impedance load in the first and second bit lines at a level that allows generation of differential signals in the bit lines. In an embodiment of the invention, the equilibration circuit comprises first and second pMOS devices in series with the first and second bitlines, respectively, and a third pMOS device connected between the first and second bitlines. The gates of the first, second and third pMOS devices are connected to the reference voltage. In this embodiment, the first, second and third pMOS devices operate as resistors in the linear region of MOSFET device operation. The memory cell bitlines can move from a sensed state "low" to the opposite state "high" without an intervening precharge, thereby providing a significant increase in performance.